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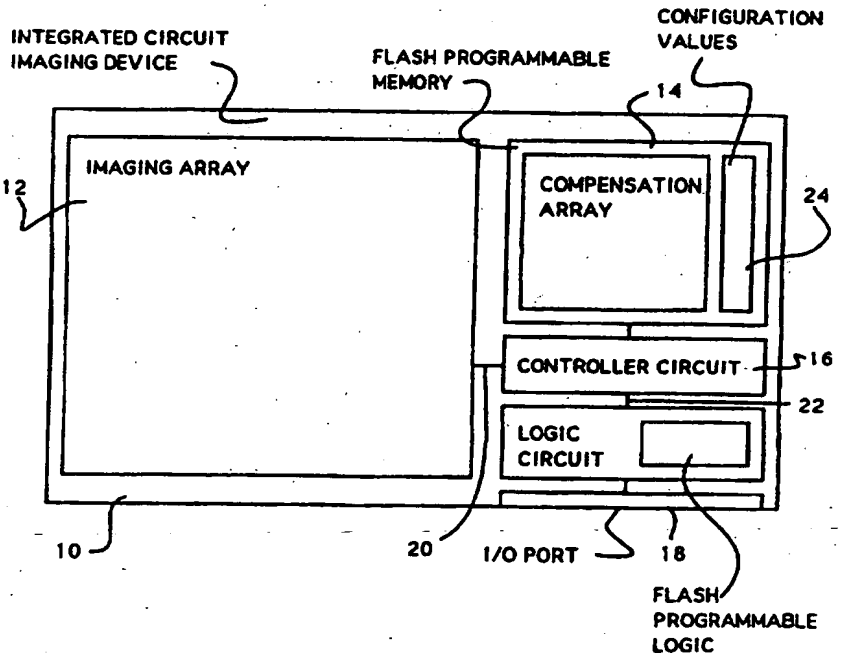
(54) Title: CMOS IMAGING DEVICE WITH INTEGRATED FLASH MEMORY IMAGE CORRECTION CIRCUITRY

(57) Abstract

A CMOS image sensing device includes, on one integrated circuit, a sensor array (12) and compensation circuitry (14) for adjusting signals output from the sensor array (12) to compensate for output signal variations, such as variations caused by voltage, temperature or process variations. The integrated circuit also includes logic circuitry (18) for performing image processing operations on signals output from the sensor array (12). The sensor array (12) is illuminated by a flat light source and variations among the magnitude of analog output signals from the elements are detected and corresponding compensation values are calculated and stored in the compensation circuitry (14). Thereafter, analog signals output from the sensor array (12) are adjusted in accordance with the compensation values.



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CMOS IMAGING DEVICE WITH INTEGRATED FLASH MEMORY IMAGE CORRECTION CIRCUITRY

BACKGROUND OF THE INVENTION

1. Field of the Invention

The invention generally relates to imaging devices and particularly to integrated circuit imaging devices requiring compensation for process and other variations.

2. Description of Related Art

Integrated circuit imaging devices include an array of light detecting elements interconnected to generate analog signals representative of an image illuminating the device. One common example of an integrated circuit imaging device is a charge coupled device (CCD) which is relatively expensive and consumes a relatively large amount of power. An alternative integrated circuit imaging device employs complementary metal oxide semiconductor (CMOS) image sensing elements. Within such an integrated circuit, a CMOS photo diode or photo transistor is employed as a light detecting element. In one example, conductivity of the element varies in accordance with the intensity of light illuminating the element. In other example, charge is collected in accordance with the intensity of light illuminating the element. By conducting current through the element or storing charge, an analog signal is thus generated having a magnitude approximately proportional to the intensity of light illuminating the element. CMOS integrated circuit imaging devices are considerably cheaper than CCD-type devices and may consume less power.

Both the CCD and CMOS integrated circuit imaging devices may require compensation for differences caused by variations within the integrated circuits, such as process, temperature, manufacturing, or voltage variations. For example, two different CCD elements within a single integrated circuit may generate analog signals of

differing magnitudes for the same intensity of light illumination. Likewise, two CMOS photo diodes or photo transistors may generate analog signals of differing magnitudes when illuminated by light of equal intensity. As such, when exposed to a flat light image having equal intensities throughout, typical CMOS or CCD arrays may output analog signals having significant magnitude variations. Accordingly, if the analog signals are used to reproduce the original image, the reproduced image will not match the original flat image but will include a significant amount of variability and noise.

To eliminate this problem, imaging devices incorporating CCDs or CMOS photo diodes or photo transistors often include a compensation system for detecting and compensating for differences among the individual imaging elements. In one arrangement, a separate integrated circuit is provided with a random access memory (RAM). The integrated circuit containing the CCD or CMOS imaging elements is exposed to a flat image. Analog signals generated therefrom are converted to digital signals and binary compensation values representative of those signals are calculated and stored within the RAM. Thereafter, during use, analog signals received from the CCD or CMOS imaging array are converted to digital signals then adjusted in accordance with the binary values stored within the corresponding RAM array to compensate for any inherent variations between the sensing elements to thereby eliminate the aforementioned variability and noise. As such, if once again exposed to flat light, analog images output from the overall system are adjusted to match the flat input image.

Typically, such systems include, in addition to the integrated circuit imaging array and the separate RAM array, a separate controller circuit and a separate image processing logic circuit. The controller circuit controls generation of the compensation values for storage within the RAM array and the application of those values for adjusting subsequent images. The controller may also provide timing signals for the proper clocking of the imaging array. The image processing logic may include, for example, logic for filtering the image

or otherwise manipulating the image to perform pattern recognition and the like.

Thus, typical integrated circuit imaging devices often include separate integrated circuits for the imaging array, the RAM, the compensation controller and the image processing logic. The provision of separate integrated circuits for the various components, and corresponding separate packaging elements, results in a fairly high cost for the overall system. Moreover, the need to transmit signals from one integrated circuit to the other can result in a relatively slow processing times, particularly for imaging arrays having a large number of elements such as a 1024-by-1024 array and higher.

It would be desirable to provide an improved integrated circuit imaging system which overcomes these disadvantages.

SUMMARY OF THE INVENTION

In accordance with one aspect of the invention, an integrated circuit imaging device is provided with a sensor array, a flash programmable memory array, and a controller circuit for controlling operation of the sensor array and the flash programmable memory array, with the sensor array, the memory array and the controller circuit all formed on a single integrated circuit chip.

In one embodiment, the integrated circuit is formed using a CMOS process. The sensor array is composed of a plurality of individual CMOS photo diode or photo transistor elements. The flash programmable memory array is composed of a plurality of individual memory storage locations each capable of storing a binary value sufficient to accommodate a compensation value. The controller circuit is connected to the sensor array and to the flash programmable memory array. The controller circuit includes circuitry for receiving analog signals from the sensor array responsive to a flat image illumination, or other known image, and for generating compensation values therefrom. The controller circuit also includes

circuitry for flash programming the memory array to store the compensation values. Moreover, the controller circuitry includes circuitry for receiving signals corresponding to subsequent images illuminating the sensor array and for adjusting the signals in accordance with the compensation values stored within the flash programmable memory array for outputting a compensated set of signals.

In the exemplary implementation, the single integrated circuit also includes a logic circuit for processing or manipulating the set of signals output from the controller circuit to, for example, perform pattern recognition or the like. The single IC also provides timing signals for the proper clocking of the imaging array.

In accordance with another aspect of the invention, a single integrated circuit imaging device is provided wherein individual CMOS imaging elements, such as photo diodes or photo transistors, are directly flash programmed to achieve direct compensation. As with the exemplary embodiment above, the single integrated circuit is provided with a sensor array of CMOS photo diodes or photo transistors and a controller circuit for receiving signals from the imaging array and for generating compensation values therefrom. However, rather than providing a separate flash programmable memory array for storing the compensation values, the controller circuit applies the compensation values to directly flash program the CMOS photo diodes or photo transistors.

In one example, each individual CMOS imaging element is an active photo diode device having a photo diode, a drive transistor and a multiplexer. A gate of the drive transistor is connected to an output of the multiplexer. A first input of the multiplexer is connected to the photo diode. A second input of the multiplexer is connected to the controller circuit. The multiplexer is controlled by a selection signal provided by a selection line also connected to the controller circuit. For flash programming of the device, the multiplexer is controlled to select the input from the control circuit which provides a voltage signal sufficient to perform flash programming of the gate of the drive

transistor, perhaps by hot-ion injection. The flash programming of the drive transistor causes a change in the electrical characteristics of the drive transistor to change the strength of the drive transistor by an amount proportional to the compensation value determined for that imaging element. Thereafter, the multiplexer is controlled to direct signals from the photo diode to the gate of the drive transistor. Current drawn by the drive transistor is therefore modulated by the intensity of light illuminating the photo diode with automatic and immediate compensation. In other embodiments, passive CMOS photo detection elements may be employed.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a block diagram illustrating a CMOS integrated circuit imaging device configured in accordance with a first exemplary embodiment of the invention.

Figure 2 is a flowchart illustrating a method for processing images using the integrated circuit imaging device of Figure 1.

Figure 3 is a block diagram of an alternative integrated circuit imaging device.

Figure 4 is a circuit schematic of a passive photo diode sensor element for use with the integrated circuit of Figure 3.

Figure 5 is a circuit schematic of an active photo gate sensor element for use with the integrated circuit of Figure 3.

Figure 6 is a circuit schematic of an active photo diode sensor element for use with the integrated circuit of Figure 3.

Figure 7 is a flowchart illustrating a method for processing images using the integrated circuit imaging device of Figure 3.

DETAILED DESCRIPTION OF EXEMPLARY EMBODIMENTS OF THE INVENTION

With reference to the remaining figures, exemplary embodiments of the invention will now be described. The exemplary

embodiments are described primarily with reference to block diagrams and flowcharts. As to the flowcharts, each block within the flowcharts represents both the method step and an apparatus element for performing the method step. Herein, the apparatus element may be referred to as a means for, an element for, or a unit for performing the method step. As to the block diagrams, it should be appreciated that not all components necessary for a complete implementation of a practical system are illustrated or described in detail. Rather, only those components necessary for a thorough understanding of the invention are illustrated and described. Furthermore, components which are either conventional or may be readily designed and fabricated in accordance with the teachings provided herein are not described in detail.

Figure 1 illustrates a single integrated chip 10 formed from a CMOS process and having an image sensor array 12, a flash programmable RAM array 14, a controller unit 16 and a logic unit 18. Sensor array 12 includes a grid of individual CMOS light sensing elements configured to output analog signals representative of an amount of light intensity illuminating the elements to controller 16 along an analog signal connection bus 20. Depending upon the configuration, analog signals from elements of array 12 may be output simultaneously in parallel, output one at a time in series, or output row-by-row or column-by-column, etc. Controller circuitry includes analog-to-digital (A/D) circuitry, not separately shown, for converting analog signals received from sensor array 12 to digital signals. The digital signals are routed along a digital bus line 22 to logic unit 18 for further processing. Logic unit 18, depending upon the configuration, performs one of a wide variety of image processing operations including, for example, pattern recognition operations, filtering operations, Fourier transform operations, and the like.

Resulting digital signals are output from circuit 10 through a digital I/O port 22. Depending upon the implementation, the content and format of the digital output signals may differ. For many applications, it may be desirable to output an entire input image,

perhaps filtered, in digital form. In other words, one digital value is output for each corresponding element of sensor array 12. In other implementations, it may be desirable to output only digital values resulting from operations performed by the logic circuit on the image detected by array 12. For example, for a pattern recognition application, it may be desirable to output signals identifying whether a particular pattern is recognized or not. In still other applications, it may be desirable to output compressed versions of the detected image. For example, although sensor array 12 may provide a 1024-by-1024 array of elements, logic unit 18 may output digital values corresponding to only a 512-by-512 compressed array. As can be appreciated, a wide range of digital output signals and formats may be employed corresponding to a wide range of functions or operations that may be performed by logic circuit 18. For most applications, logic unit 18 is preconfigured to perform only one particular operation on the detected image. In other embodiments, however, the logic unit may be configured to perform one of several operations with the particular operation being selected by an input signal received from I/O port 22.

Flash memory array 14 includes an array of individual memory locations for storing compensation values for corresponding elements of sensor array 12. For example, if sensor array 12 is 1024-by-1024 array, then flash memory 14 includes a 1024-by-1024 array of storage locations for storing compensation values. Depending upon the implementation, each compensation value may be 4 bits, 8 bits, etc. The choice of the number of bits for each compensation value depends upon the desired precision for compensation. In some implementations, each compensation value may be only 2 or 3 bits.

The arrangement of compensation values within flash memory 14 may be entirely arbitrary so long as each compensation value can be matched with a corresponding element of the sensor array. In other words, whereas the sensor array requires a physically 2-dimensional layout to allow a 2-dimensional image to be detected, the flash

memory does not require any corresponding 2-dimensional physical layout.

In use, sensor array 12 is exposed to a flat light field or a field of known light intensity variation. Signals generated by the sensor element are transmitted to controller 16 which calculates compensation values in response thereto. The calculation of compensation value may be entirely in accordance with conventional techniques. Controller 16 then transmits the compensation values to flash memory 14 for flash programming therein, perhaps using hot-ion injection techniques. Again, such can be in accordance with conventional techniques. Depending upon the implementation, actual flash programming of array 14 may require an iterative programming process whereby elements are programmed, then tested to determine whether the correct values are programmed and, if not, reprogrammed. Thereafter, integrated circuit 10 operates in the manner described above wherein sensor array 12 is exposed to an image and controller 16 adjusts signals output from the sensor array in accordance with corresponding compensation values from the flash memory array. Flash programming of the memory array is preferably performed at a factory following fabrication of the integrated circuit. However, in other circumstances, it may be desirable for customers to flash program the memory cells.

Figure 2 is a flowchart summarizing the above-described method for operating integrated circuit 10. Initially, at step 50, the sensor array of the integrated circuit is illuminated by a flat image. Next, at step 52, the controller circuit calculates compensation values for each of the pixels of the sensor array for use in eliminating variations in output signals from the pixels. Next, at step 54, the RAM array is flash programmed to record the compensation values. Thereafter, at step 56, the sensor array is illuminated by a subsequent image which may be, for example, an image subject to pattern recognition. At step 58, the controller circuit adjusts individual signals received from the sensor array with corresponding compensation values from the RAM array to generate an adjusted set

of signals and thereby substantially eliminate noise from the detected image represented by the signals.

Referring again to Figure 1, thus far, an integrated circuit has been described wherein a portion of the circuit is employed as flash memory for storing compensation values. Additionally, however, other portions of the circuit may be employed as flash memory for storing other values as well. For example, portions of memory 14 may be employed for storing configuration values perhaps directed towards particular applications. For example, if the integrated circuit is intended for use within a video camera, then certain configuration values useful in such an application are stored within the flash memory. On the other hand, if the integrated circuit is intended for use within a medical imaging device, then alternative configuration values are stored. As can be appreciated, a wide range of values may be flash programmed to facilitate a wide range of applications. In Figure 1, a portion of flash memory 14, identified by reference numeral 24, stores such configuration values.

Other portions of the integrated circuit may be flash programmed as well. For example, portions of logic circuit 18 may be flash programmed to perform specific operations directed towards particular applications. For pattern recognition operations, for example, certain patterns to be recognized may be flash programmed into a portion of the logic circuit or into a secondary memory (not separately shown) connected thereto. In other implementations, logic circuit 18 may be capable of performing a number of different operations and portions thereof are flash programmed to select one of the specific operations. Within Figure 1, a portion of logic circuit 18 subject to flash programming is identified by reference numeral 26.

Thus, other portions of integrated circuit 10 besides flash memory 14 may be flash programmed as needed. Indeed, even sensor array 12 may be flash programmed. In the following, embodiments are described wherein individual elements of a sensor array are flash programmed to perform direct compensation without requiring a separate flash memory storing compensation values. This

embodiment is illustrated in Figures 3-7. Figure 3 illustrates an alternative integrated circuit to that of Figure 1. The circuit of Figure 3 is similar to that of Figure 1 and like components are represented by like reference numerals incremented by 100. Only pertinent differences between the embodiments will be described.

Figure 3 illustrates the integrated circuit 110 having a sensor array 112, a controller circuit 116 and a logic circuit 118. Sensor array 112 includes a 2-dimensional array of individual sensor elements having drive transistor devices directly flash programmed by controller circuit 116 to perform direct compensation. As such, a separate flash memory array is not required. In all other respects, integrated circuit 110 may operate in the same manner as integrated circuit 10.

Depending upon the implementation, the individual photo detecting elements of sensor array 112 may differ. Figures 4-6 illustrate examples of CMOS photo detection elements that may be appropriate for various applications. Figure 4, for example, illustrates a passive pixel photo detection element 200 having a photo diode 202 and an NMOS drive transistor 204. Transistor 204 is connected between photo diode 202 and an output line 206. A gate of transistor 204 is connected to the output of the multiplexer 208 which receives either a row strobe signal along a line 210 or a flash programming compensation signal along line 212. Multiplexer 208 is controlled by a selection signal along select line 214. Lines 210, 212 and 214 are all connected to the controller circuit. In use, to flash program the pixel element, the controller circuit transmits a signal along line 214 selecting the input from 212 then transmits a programming voltage along line 212 to program transistor 204. The gate of transistor 204 is physically modified by the programming voltage to modify the electrical characteristics of the transistor to reduce its drive strength by an amount sufficient to compensate for variations in photo diode 202. Thereafter, mutliplexer 208 is controlled to receive signals along line 210 for selecting the photo diode during use via a conventional row strobe signal.

Figure 5 illustrates an active pixel arrangement employing a photo gate light detection element subject to flash programming. More specifically, Figure 5 illustrates a pixel element 300 having a photo gate 302 and a set of NMOS transistors 304, 306, 308 and 310 connected as shown. Transistor 306 is connected between a voltage source VDD and a selection transistor 308 and operates as a drive transistor. Drive transistor 306 is a gate connected to the output of a multiplexer 312. When input of the multiplexer is connected to an output of photo diode 302 along a line 314 another input is connected to the controller circuitry along line 316 for receiving a flash programming signal. Multiplexer 312 is controlled by a selection signal provided along a selection line 318 also connected to the controller circuitry. As with the passive pixel arrangement of Figure 4, the multiplexer of the photo gate arrangement of Figure 5 is controlled to transmit a flash programming signal to a gate of drive transistor 306 to alter the electrical characteristics of the drive transistor to achieve compensation. Thereafter, the multiplexer is controlled to transmit output signals from the photo diode to the gate of the drive transistor which controls generation of an output signal for transmission to the controller circuitry along an output line 320.

Figure 6 illustrates an active pixel arrangement employing a photo diode rather than a photo gate. More specifically, Figure 6 illustrates a photo diode pixel element 400 having a photo diode 402 and a set of three NMOS transistors 404, 406 and 408. NMOS transistor 406 operates as a drive transistor. As with the arrangement of Figure 5, a gate of the drive transistor is connected to the output of the multiplexer which receives, along one input, an output from the photo diode and receives along another input, a flash programming signal from the controller circuit. The multiplexer is controlled by a selection signal also received from the controller circuit. The active photo diode arrangement of Figure 6 operates similarly to the active photo gate arrangement of Figure 5 and such operation will not be redescribed.

Figure 7 is a flowchart summarizing the operation of the integrated circuit of Figure 3. Initially, at step 500, the sensor array is illuminated by a flat light image. Next, at step 502, the controller circuit calculates compensation values, one per pixel of the sensor array, for use in compensating for differences among the output signals of the pixels. Thereafter, at step 504, drive transistors of the individual pixel elements of the sensor array are directly flash programmed to alter the electrical characteristics of the drive transistors by an amount related to the corresponding compensation values. Thereafter, at step 506, the sensor array is illuminated by a subsequent image and analog signals generated by individual pixels of the sensor array are automatically adjusted, as a result of the flash programming of the drive transistors, to provide automatic image compensation.

What has been described are various embodiments of an integrated circuit CMOS imaging detection device having all necessary components integrated onto a single circuit rather than provided on several separate chips. Compensation for variations among individual photo detection elements, such as process variations, is achieved by flash programming portions of the integrated circuit. In one arrangement, a flash memory is provided for storing compensation values. In another arrangement, drive transistors of individual photo detection elements of the sensor array are directly flash programmed to achieve direct compensation. Other arrangements are also possible consistent with the general principles of the invention.

Also although described primarily with respect to an integrated circuit having a 2-dimensional sensor array, other sensor configurations are possible. For example, in some embodiemntes, only a single sensor pixel or line of pixels may be employed. The exemplary embodiments described herein are intended merely to illustrate principles of the invention and should not be construed as limiting the scope of the invention.

CLAIMS

What is claimed is:

1. A single integrated circuit comprising:

a sensor array;

a flash programmable memory array; and

a controller circuit for controlling operation of the sensor array and the flash programmable memory array.

2. A single integrated circuit comprising:

a sensor array having a plurality of individual pixel sensor elements for outputting signals representative of input light;

a flash programmable memory array for storing compensation values for adjusting the signals; and

a controller circuit for receiving signals from the sensor array and for adjusting the signals in accordance with the compensation values stored within the flash array.

3. A single integrated circuit comprising:

sensor array means for sensing light and for outputting signals in response thereto;

flash programmable means for storing compensation values for use in adjusting the signals output from the sensor array; and

controller means for controlling operation of the sensor array and the flash programmable means.

4. The single integrated circuit of claim 3 wherein the flash programmable means comprises:

a flash programmable memory array for storing compensation values for use in compensating for noise among signals generated by the sensor array means caused by process variations in the integrated circuit.

5. The single integrated circuit of claim 3 wherein said sensor array means comprises a plurality of individual photosensitive detector circuits; and

wherein said flash programmable means includes a separate individual flash programmable compensation circuit connected to each of said individual photo diode circuits of said sensor array means, said individual flash programmable compensation circuits configured to compensate for analog signal values generated by the corresponding photo diode circuit.

6. The single integrated circuit of claim 3 wherein said controller means includes means for flash programming the flash programmable means.

7. The single integrated circuit of claim 6 wherein the means for flash programming includes:

means for receiving signal values from the sensor array means representative of a flat light image exposed to the sensor array;

means for calculating compensation values based upon differences among the signal values provided by individual pixel elements of the sensor array means; and

means for flash programming the flash programmable means based upon the calculated compensation values for use in compensating for differences among the individual pixel elements of the sensor array.

8. The single integrated circuit of claim 5 wherein each individual photo diode means include a photo diode having an input connected to a voltage source and wherein each of said individual compensation circuits includes a mutliplexer having a first input connected to an output of the corresponding photo diode and a second input connected to a flash programming voltage value, and an output connected to an output transistor of the photo diode circuit.

9. A method for processing images detected by an integrated circuit having a sensor array and a flash programmable memory array, said method comprising the steps of:

illuminating the sensor array with a known image;

analyzing responsive signals generated by the sensor array and generating compensation values therefrom;

flash programming the memory array to store the compensation values;

illuminating the sensor array with a subsequent image; and

adjusting responsive signals from the sensor array using the compensation values from the memory array.

10. The method of claim 9 wherein the known image is a flat light image.

11. The method of claim 9 wherein the step of analyzing the responsive signals and generating compensation values comprises the steps of:

comparing the responsive signals with expected signals to determine differences therebetween and generating compensation values representative of said differences.

12. A method for processing images detected by an integrated circuit having a sensor array with individual pixel elements having flash programmable drive transistors, said method comprising the steps of:

illuminating the sensor array with a known image;

analyzing responsive signals generated by the sensor array and generating compensation values therefrom;

flash programming the drive transistors of the individual pixel elements in accordance with corresponding compensation values; and

illuminating the sensor array with a subsequent image and generating signals responsive thereto, said signals being automatically

adjusted in accordance with the compensation values as a result of the direct flash programming of the drive transistors.

13. The method of claim 12 wherein the step of analyzing the responsive signals and generating compensation values comprises the steps of:

comparing the responsive signals with expected signals to determine differences therebetween and generating compensation values representative of said differences.

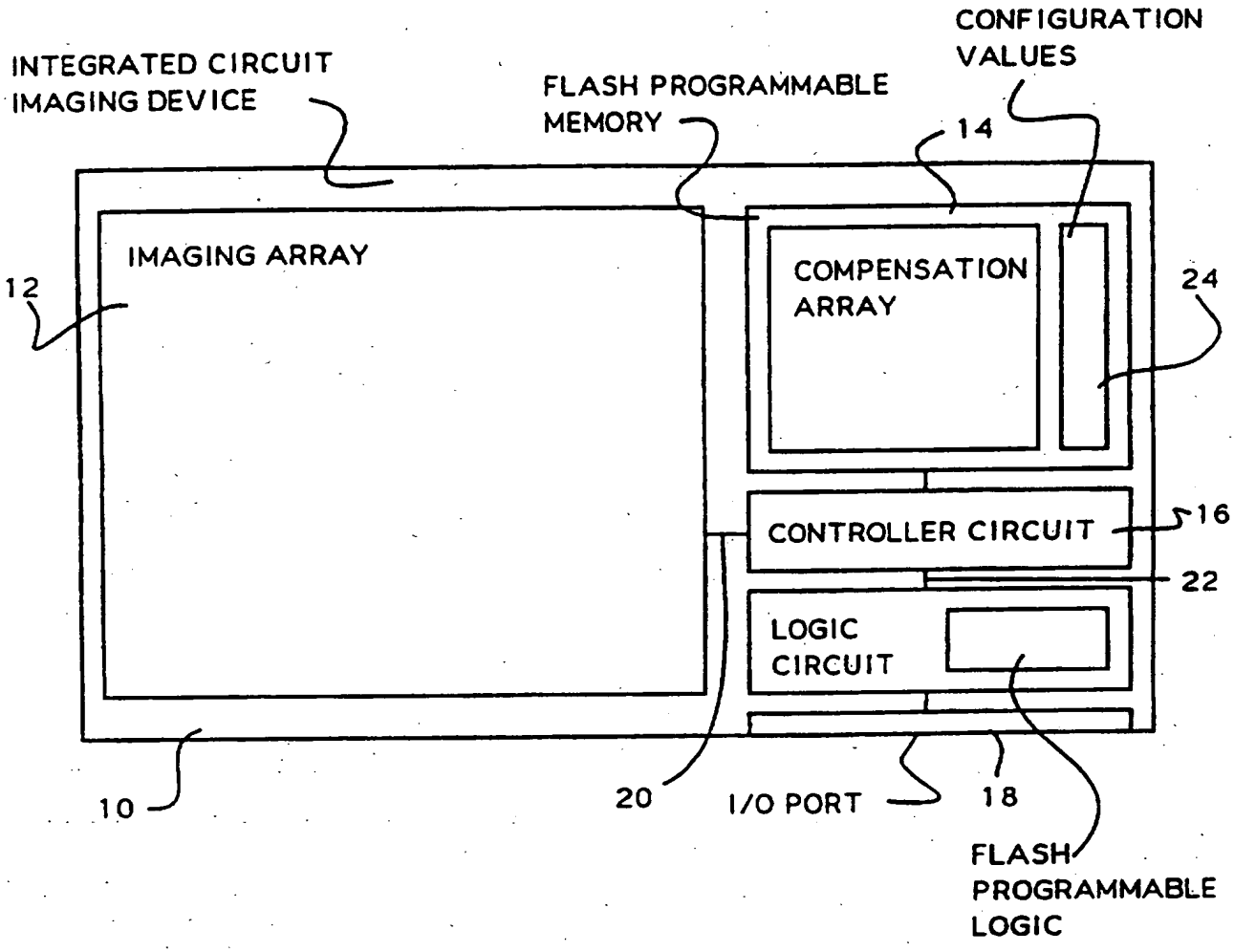

FIG. 1

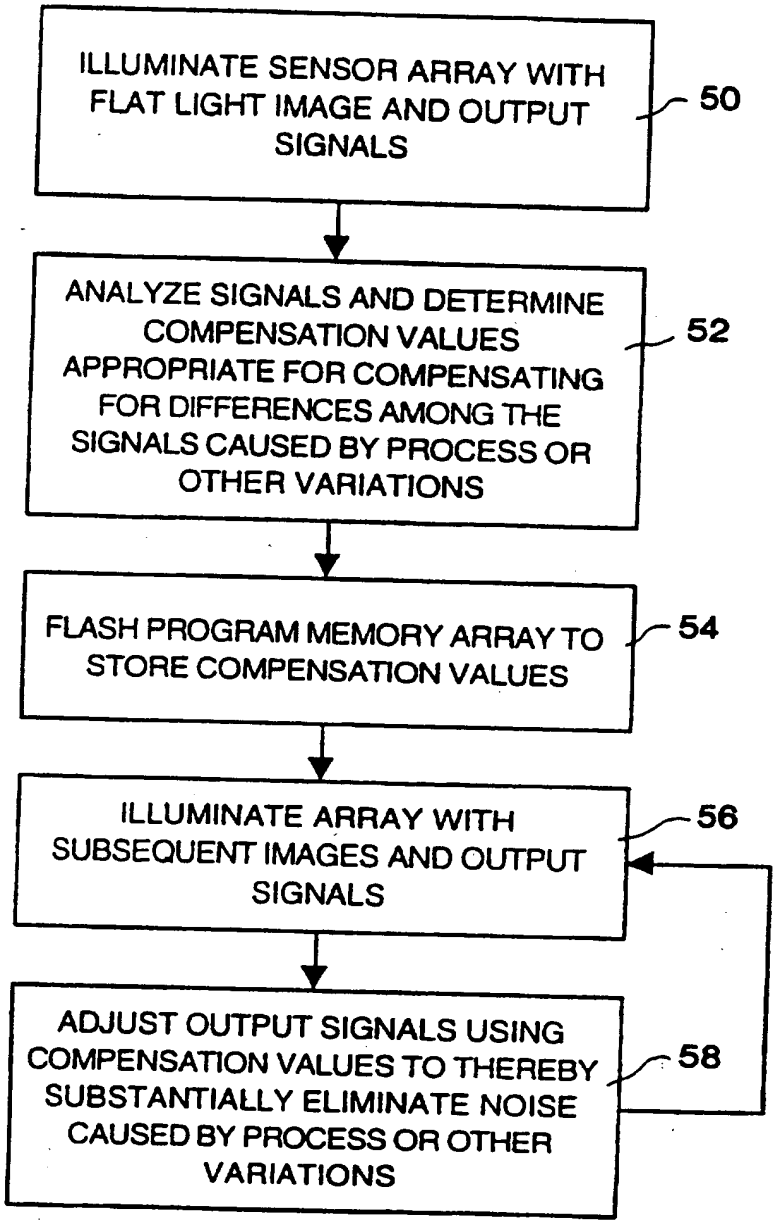

FIG. 2

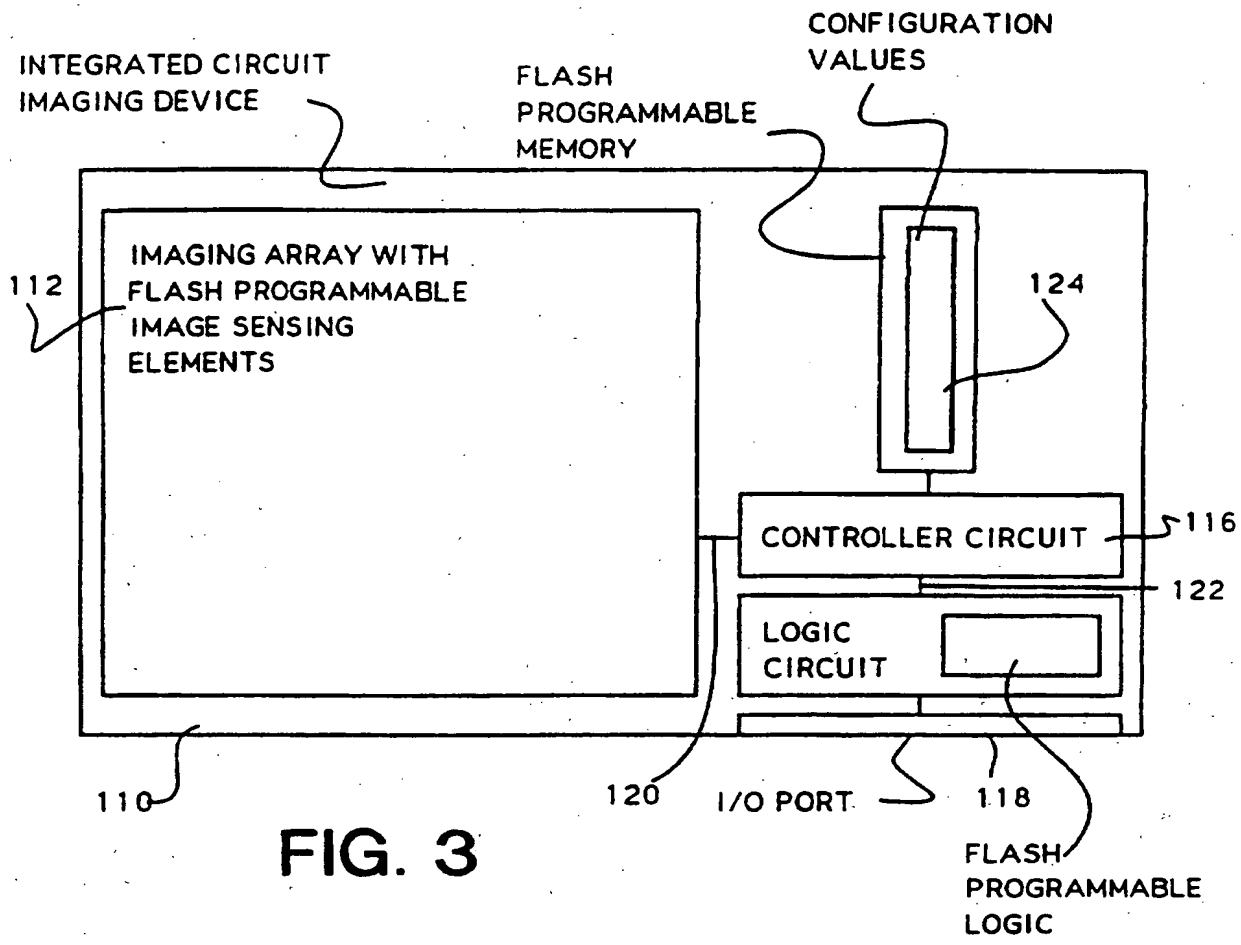

FIG. 3

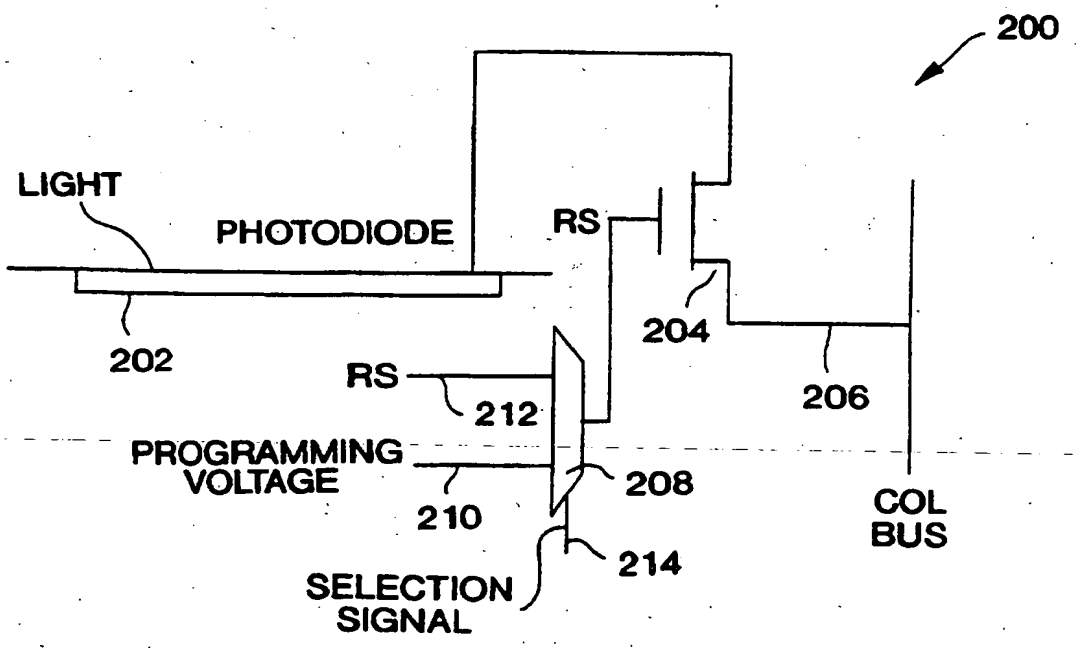

FIG. 4

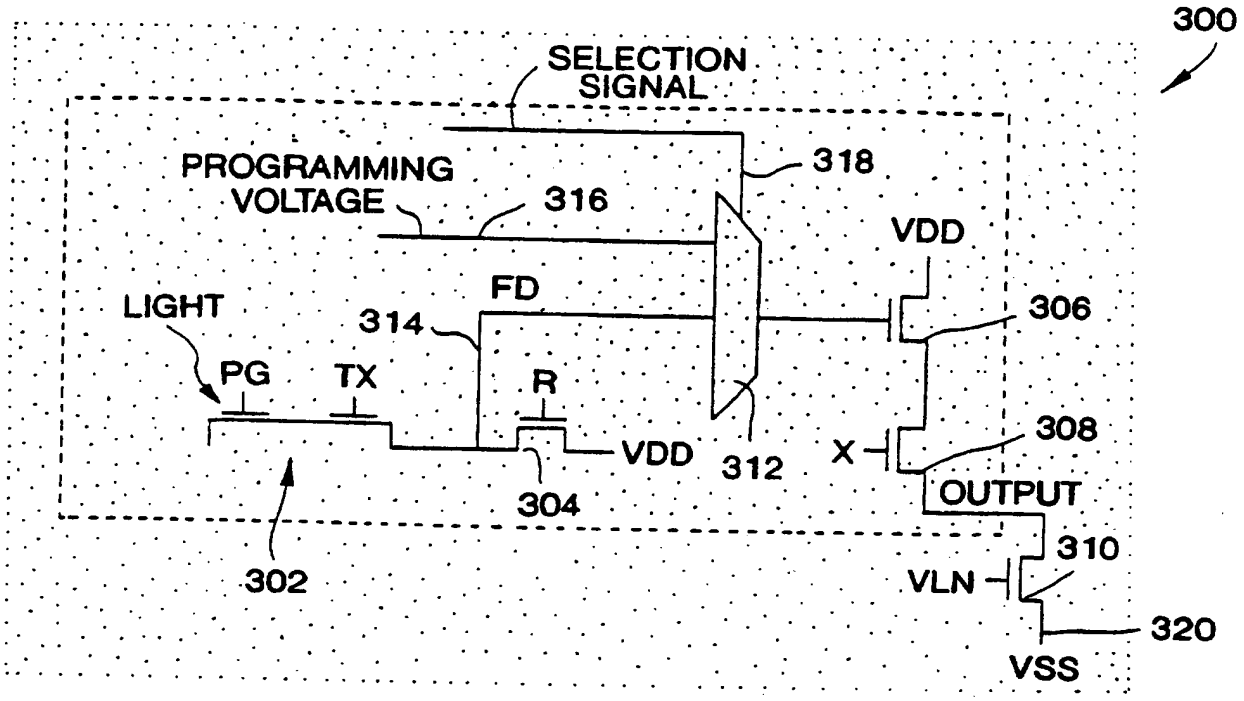

FIG. 5

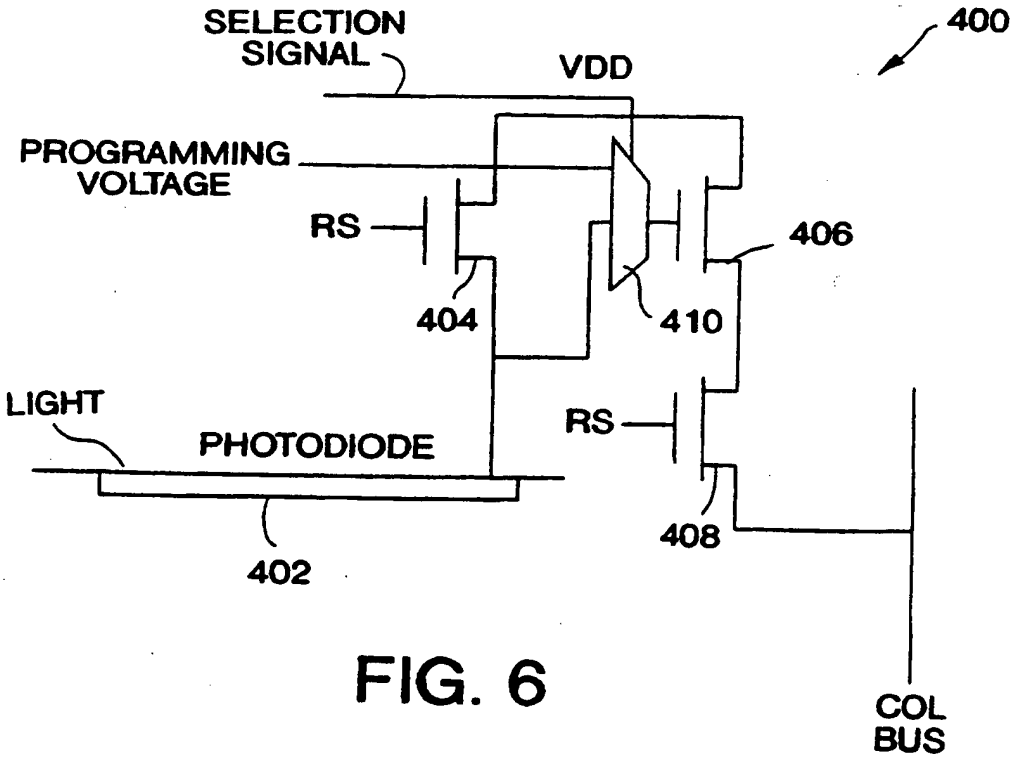

FIG. 6

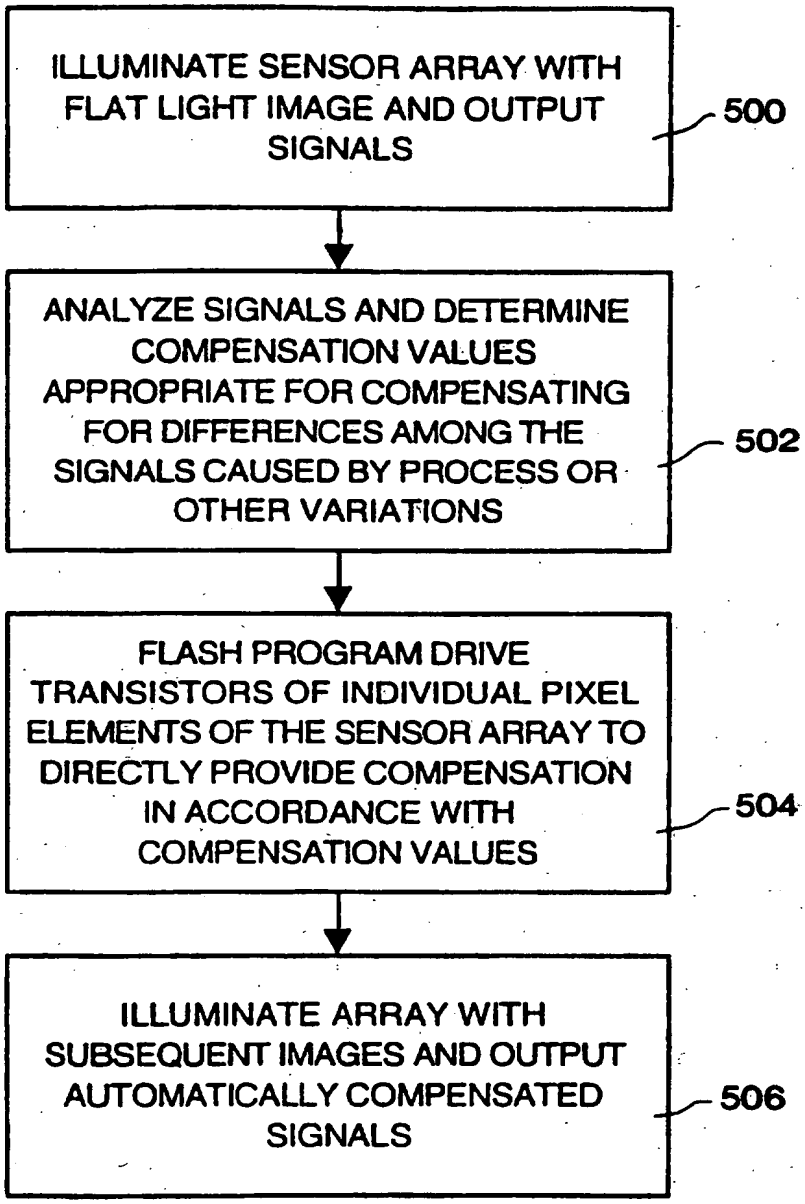

FIG. 7

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US96/20870

A. CLASSIFICATION OF SUBJECT MATTER

IPC(6) :G11C 7/00
US CL :365/ 185.03, 185.09, 185.33
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 365/ 185.03, 185.09, 185.33

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

NONE

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

NONE

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US, 5,164,603, A, (HARTMAN ET AL.) 17 NOVEMBER 1992, see entire document.	1-13
X	US, 5,247,166, A, (CANNON ET AL.) 21 SEPTEMBER 1993, see entire document	1-13

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

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